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10ES33

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Express the given expression in standard SOP form; f[A,B,C] = AC + AB + BC. **(03 Marks)**

b. Express the given expression in standard POS form; f[A,B,C] = (A + B)(B + $\overline{C}$)(A + C). **(03 Marks)**

c. A combinational logic circuit has 3 inputs, the output will be low only when majority of inputs are high ;
   i) Derive truth table
   ii) Write the POS expression
   iii) Convert the POS equation to SOP form
   iv) Simplify the expression using k-map and implement it using only NAND gates. **(14 Marks)**

2 a. Design an odd parity bit generator using gates for the decimal digits 0 to 9 represented in 8421 BCD. Give the necessary truth table and the logic diagram with the explanation. **(10 Marks)**

b. Simply the following 5 variable Boolean function using Quine –McCluskey method :
$f = \Sigma m(0, 1, 9, 15, 24, 29, 30) + d(8, 11, 31)$. **(10 Marks)**

3 a. Describe a 4-bit priority encoder with the help of truth table and k-map simplification for outputs, draw the logic circuit. **(10 Marks)**

b. Implement the following two output function using 74LS138 and external gates
$F_1(A,B,C) = \Sigma m(1,2,6,7)$
$F_2(A,B,C) = \pi M(1,3,6,7)$. **(04 Marks)**

c. Design a keypad interface to a digital system using ten line BCD encoder 74LS147. **(06 Marks)**

4 a. Implement the following Boolean function using 8 : 1 multiplexer
$F(A,B,C,D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$. **(06 Marks)**

b. State the applications of multiplexers. **(04 Marks)**

c. Design a full adder with the help of truth table and implement it with basic gates. **(10 Marks)**

PART – B

5 a. Distinguish between combinational circuit and sequential circuits with an example to each. **(04 Marks)**

b. Explain the operation of master-slave J-K flip-flop with NAND gate circuit and input output waveforms. **(10 Marks)**

c. Explain the working of switch debouncers using S-R latch. **(06 Marks)**

6 a. Describe the different modes of operation of shift registers. **(04 Marks)**

b. What are the applications of shift register? **(04 Marks)**

c. Describe a 4-bit synchronous binary counter with a block diagram and timing diagram. **(12 Marks)**

7 a. Describe a Moore model with an example. **(06 Marks)**

b. Design a synchronous mod-6 counter using JK flip-flop with the excitation table and k-map simplification, determine the transition table. **(14 Marks)**

8 a. A sequential circuit has one input and one output. The state diagram is shown in Fig.Q8(a). Design a sequential circuit with D-flip-flop. **(12 Marks)**

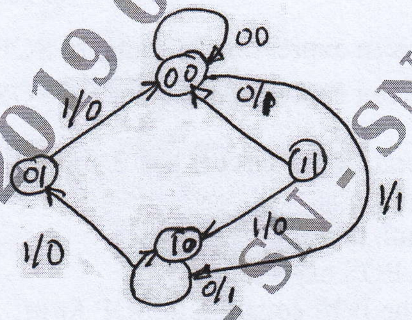

Fig.Q8(a)

b. State the steps for the design of a clocked synchronous sequential circuit. **(08 Marks)**

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